IN THE SPECIFICATION:

Please amend the specification as follows:

(1) The paragraph from page 3, line 2 to page 3, line 14 has been amended as follows:

The assignee of this invention has proposed a new type of test system which is an event based test system wherein the desired test signals and strobe signals are produced by event data from an event memory directly on a per pin basis. In the event based test system, the event timing and event repetition rate can be freely modified by an event offset function and an event scaling function. The conventional characterization tools noted above are insufficient to fully ~~utilized~~ utilize the capability of the event test system. Thus, there is a need of new characterization tools in the event based test system to fully illustrate the device characteristics utilizing the new functions of the event based test system.

(2) The paragraph from page 5, line 2 to page 5, line 7 has been amended as follows:

Figures 5A and 5B are schematic diagrams showing examples of semiconductor characterization map of the present invention where Figure 5A is a margin map showing a timing relationship between a device output and strobe signals and Figure 5B is a timing diagram showing the waveforms defined in ~~Figure 5~~ Figure 5A.

(3) The paragraph from page 5, line 9 to page 5, line 16 has been amended as follows:

In the previous applications owned by the same assignee of this invention, an event based test system is described in U.S. Patent Application Nos. 09/406,300 (now U.S. Patent No. 6,532,561) and 09/340,371 (now U.S. Patent No. 6,678,643) "Event based semiconductor test system". Further, a time scaling technology is described in U.S. Patent Application No. 09/286,226 (now U.S. Patent No. 6,557,133) "Scaling logic for Event Based Test System". All of these patent applications are incorporated by reference.

(4) The paragraph from page 6, line 11 to page 6, line 20 has been amended as follows:

As described in the prior applications, the event data formed in the event file directly describes the test pattern to be applied to the device under test. Therefore, with use of the event data, through graphic user interface (GUI), the pattern sequence identical to the actual test pattern can be displayed. Such a pattern sequence can be easily modified through the graphic display. Thus, device characterization maps of various parameters are available in the present invention. An example of such characterization maps is shown in Figure 1 by screens 81-85.

(5) The paragraph from page 6, line 29 to page 7, line 3 has been amended as follows:

The screens 84 and 85 show the scaling function in which the timings are decreased (84) or increased (85) by a predetermined ~~**factor,**~~ factor. Such changes in the parameters on the display can be done by modifying the data in the event file, which also changes the actual test pattern applied to the device under test and thus enables to monitor the resultant response of the device under test. The more details regarding the scaling of the timing data is given in U.S. Patent Application No. 09/286,226 (now U.S. Patent No. 6,557,133) and U.S. Patent No. 6,226,765 owned by the same assignee of this invention.

(6) The paragraph from page 7, line 20 to page 7, line 31 has been amended as follows:

Another function of the event based test system is the timing offset such as shown in the screen 83. ~~**The**~~ In this function, the timing of the event (drive event, compare event) is changed ~~**by**~~ for each pin and pin group. This function enables all timing edges to be shifted by the same amount for the entire run time of a pattern. A few examples, which employ this capability, are generation of characterization data to find either the slowest response in a series of device outputs, or the longest set up time in a series of input writes to a memory or programmable logic device. This function also enables a timing edge of only a specific event

be shifted by a specified amount or even be deleted from the test pattern.

(7) The paragraph from page 10, line 17 to page 10, line 28 has been amended as follows:

Figures 5A and 5B show another example of semiconductor characterization map of the present invention. Figure 5A is a margin map showing a timing relationship between a device output and compare events (strobe signals) and ~~**Figure 6B**~~ Figure 5B is a timing diagram showing the waveforms of ~~**Figure 5**~~ Figure 5A. The margin map can be used to find the pass/fail range for individual pins or pin groups corresponding with one or more events. The margin map tool applies the timing offset function of a pin or pin group to find the pass/fail of interest. The current programmed value is noted on the display, allowing the user to see how close the device is to the pass/fail threshold.